REMARKS

Claims 2, 5, 6 and 9-11 are pending in the present application. Claims 2, 5 and 6 have been amended. Claims 9-11 have been presented herewith. Claims 1, 3, 4, 7 and 8 have been canceled.

Drawings

Applicant notes the Examiner's acceptance of the drawings as filed along with the present application on August 26, 2003.

Disclosure

The disclosure has been objected to in view of the informality as listed on page 2 of the current Office Action dated February 18, 2005. The specification has been corrected as requested by the Examiner. The Examiner is therefore respectfully requested to withdraw the objection to the disclosure.

Claim Objections

Claims 1 and 8 have been objected to in view of the informalities as listed on page 2 of the current Office Action. Claims 1 and 8 have been canceled. Accordingly, the Examiner is respectfully requested to withdraw the objection to the claims.

Claim Rejections-35 U.S.C. 102

Claims 1 and 5 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Sugasawara reference (U.S. Patent No. 6,043,672). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The system large scale integration (LSI) of claim 9 includes in combination first, second and third circuit blocks; a first power supply terminal "located on the wafer and supplied with a first power supply voltage for test, wherein the first power supply voltage has a first voltage level and has a second voltage level which is different from the first voltage level"; a first power supply line "located on the wafer, which surrounds the first, second and third blocks, and which is connected to the first power supply terminal and the first and second circuit blocks"; a second power supply terminal "located on the wafer and supplied with a second power supply voltage for test, wherein the second power supply voltage has the first voltage level and has a third voltage level which is different from the first and second voltage levels"; and a second power supply line "located on the wafer, which surrounds the first, second and third circuit blocks, and which is connected to the second power supply terminal and the third circuit block". Applicant respectfully submits that the Sugasawara reference as relied upon by the Examiner does not disclose these features.

The Examiner has relied primarily upon Fig. 1 of the Sugasawara reference as meeting the features of the claims. However, as described in columns 4-5 of the Sugasawara reference and as may be readily understood in view of Fig. 1, a first power

supply pad 30 provides a power supply VDD to sections 12, 14 and 16 in region 18; a separate second power supply pad 28 provides a power supply VDD2 to the sections 12-16; and a separate third power supply pad 26 provides power supply VDD1 to sections 12-16. Integrated circuit 10 in Fig. 1 of the Sugasawara reference does not include a first power supply terminal "supplied with a first power supply voltage for test, wherein the first power supply voltage has a first voltage level and has a second voltage level which is different from the first voltage level", as would be necessary to meet the features of claim 9. That is, none of the power supply pads in Fig. 1 of the Sugasawara reference is supplied with a power supply voltage for test that has different first and second voltage levels. Applicant therefore respectfully submits that the system large scale integration (LSI) of claim 9 distinguishes over the Sugasawara reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 5 and 9, is improper for at least these reasons.

With further regard to this rejection, the Sugasawara reference as relied upon by the Examiner also fails to disclose a second power supply terminal "supplied with a second power supply voltage for test, wherein the second power supply voltage has the first voltage level and has a third voltage level which is different from the first and second voltage levels", as would be necessary to meet the further features of claim 9. Also, integrated circuit 10 in Fig. 1 of the Sugasawara reference does not disclose respective first and second power supply lines connected as featured, that surround first, second and third circuit blocks, as would be necessary to meet the further features

of claim 9. Applicant therefore respectfully submits that the system large scale integration (LSI) of claim 9 distinguishes over the Sugasawara reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 5 and 9, is improper for at least these additional reasons.

Claim Rejections-35 U.S.C. 103

Claims 2, 3, 6 and 7 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Sugasawara reference, in view of the Rostoker et al. reference (U.S. Patent No. 5,489,538). However, the Rostoker et al. reference as particularly relied upon by the Examiner does not overcome the above noted deficiencies of the Sugasawara reference. Accordingly, Applicant respectfully submits that claims 2 and 6 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection is improper for at least these reasons.

Claims 4 and 8 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Sugasawara reference in view of the Rostoker et al. reference, and in further view of the Kokado reference (U.S. Patent No. 5,072,274). Claims 4 and 8 have been canceled. The Examiner is therefore respectfully requested to withdraw this rejection for at least these reasons.

Claims 10 and 11

Applicant respectfully submits that claims 10 and 11 distinguish over and would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, at least by virtue of dependency upon claim 9, and by further reason of the features therein.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

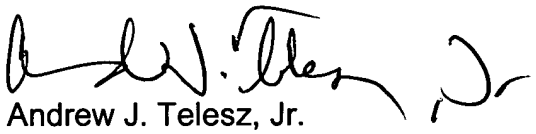
In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of one (1) month to June 18, 2005, for the period in which to file a response to the outstanding Office Action. The required fee of $120.00 should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



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